WHAT IS CLAIMED IS:

1. An insulating gate type semiconductor device comprising:

a plurality of trench gate electrodes provided substantially in parallel,

wherein among said trench gate electrodes, a thinning-out trench gate electrode excluding a channel-forming trench gate electrode is insulated from a gate wire and is connected to an emitter electrode or to predetermined electric potential generating means for generating a negative electric potential with respect to an emitter potential.

2. An insulating gate type semiconductor device comprising:

a plurality of trench gate electrodes provided in a plurality of trenches arranged substantially in parallel and each recessed to a predetermined depth extending to an upper portion of an N-type base layer from the surface of a semiconductor substrate on which a P-type emitter layer, said N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof,

wherein said trench gate electrodes are defined as channel-forming trench gate electrodes for forming a channel,

one set of said trench gate electrodes is constituted by twos arranged in sequence, and

the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a tip of said channel-forming trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and that a curvature of said depletion layer at the tip of said trench gate electrode is relieved.

3. An insulating gate type semiconductor device comprising:

a plurality of trench gate electrodes provided in a plurality of trenches arranged substantially in parallel and each recessed to a predetermined depth extending to an upper portion of an N-type base layer from the surface of a semiconductor substrate on which a P-type emitter layer, said N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof,

wherein said trench gate electrodes are defined as channel-forming trench gate electrodes for forming a channel,

one set of said trench gate electrodes is constituted by twos arranged in sequence, and

the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3μm or under.

4. An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof:

a plurality of trenches arranged substantially in parallel and each recessed to a depth extending from the surface of said semiconductor substrate to an upper portion of said N-type base layer;

a gate oxide layer provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes, with one set of said trench gate electrodes being constituted by a predetermined number, four or more, of said electrodes

arranged in sequence, among said one set of electrodes said two trench gate electrodes disposed at both side ends being structured as channel-forming trench gate electrodes connected to said gate wires, and said remaining electrodes interposed between said two channel-forming trench gate electrodes being structured as thinning-out trench gate electrodes insulated from said gate wires;

an N-type emitter layer provided on the surface of said semiconductor substrate of said P-type base layer interposed between said channel-forming trench gate electrode belonging to said one set of electrodes and said channel-forming trench gate electrode belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said channel-forming trench gate electrode;

a polysilicon layer, provided covering some portions and the whole of the upper surfaces of said thinning-out trench gate electrodes for said every set of electrodes, for connecting said thinning-out trench gate electrodes to each other which belong to said one set of electrodes;

an insulating oxide layer provided covering a part or the whole of said channel-forming trench gate and a part of said polysilicon layer, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer and at a potion provided with said polysilicon layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer, said N-type emitter layer and said polysilicon layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate.

5. An insulating gate type semiconductor device according to claim 4, wherein said gate wire is formed with a first width at a portion provided with said channel-forming trench gate electrode, and a second with smaller than the first width at a portion provided with said

thinning-out trench gate electrode.

6. An insulating gate type semiconductor device according to claim 4, wherein said thinning-out trench gate electrode and a side end of said trench provided with said thinning-out trench gate electrode on the side of said gate wire, are so formed as to be spaced away from said gate wire, and

said gate wire is formed with a fixed width.

Sub A1 7. An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof:

a plurality of trenches arranged substantially in parallel and each recessed at a first distance and a second distance alternately to a depth extending from the surface of said semiconductor substrate to an upper portion of said N-type base layer;

a gate oxide layer provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire, with one set of said trench gate electrodes being constituted by twos arranged in sequence at the first distance;

an N-type emitter layer provided on the surface of said semiconductor substrate of said P-type base layer interposed between said trench gate electrode belonging to said one set of electrodes and said trench gate electrode belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate

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electrode;

an insulating oxide layer provided covering a part or the whole of said trench gate, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate,

wherein the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a tip of said trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and that a curvature of said depletion layer at the tip of said trench gate electrode is relieved.

8. An insulating gate type semiconductor device according to claim 7, wherein the first distance is a longer than the second distance.

9. An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof:

a plurality of trenches arranged substantially in parallel and each recessed at a first distance and a second distance alternately to a depth extending from the surface of said semiconductor substrate to an upper portion of said N-type base layer;

a gate oxide layer provided on an inner surface of each of said trenches and on the surface of said

semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire, with one set of said trench gate electrodes being constituted by twos arranged in sequence at the first distance;

an N-type emitter layer provided on the surface of said semiconductor substrate of said P-type base layer interposed between said trench gate electrode belonging to said one set of electrodes and said trench gate electrode belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate electrode;

an insulating oxide layer provided covering a part or the whole of said trench gate, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate,

wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3μm or under.

10. An insulating gate type semiconductor device according to claim 9, wherein the first distance is a longer than the second distance.

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